Serial ATA について

2004.2.17
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SerialATA の特長

ATAとのソフトウェア完全互換 (容易な移行)

Embedded Clocking、8B10B coding

2 pair 差動伝送による少ない信号ピン数

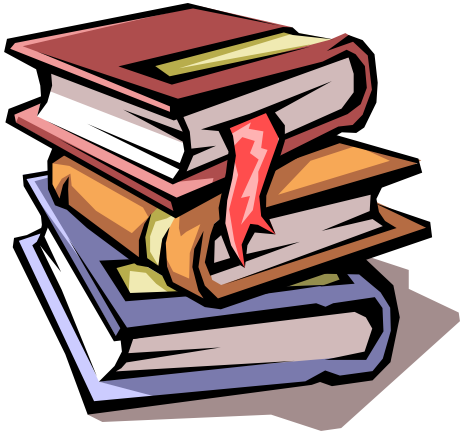
Hot Plugのサポート

ATA との等価で安価な価格体系の維持

(セラミック発振子の利用も考慮)

ATA伝送(150MB/s)以上の高速性

10年以上のroadmap



SATAの用途

PCの内蔵ディスク

ラップトップの内蔵ディスク、ドッキングステーション

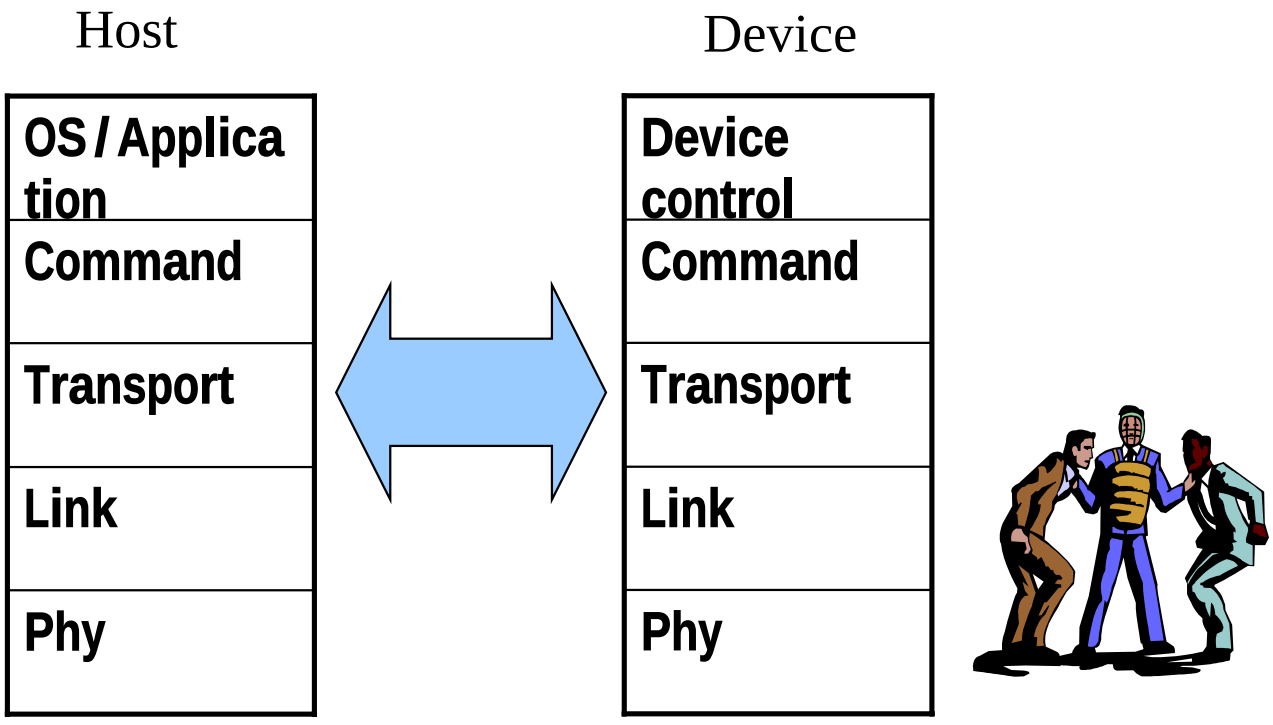
サーバの内蔵ディスク、スワップベイ

外部ドライブ、JBOD

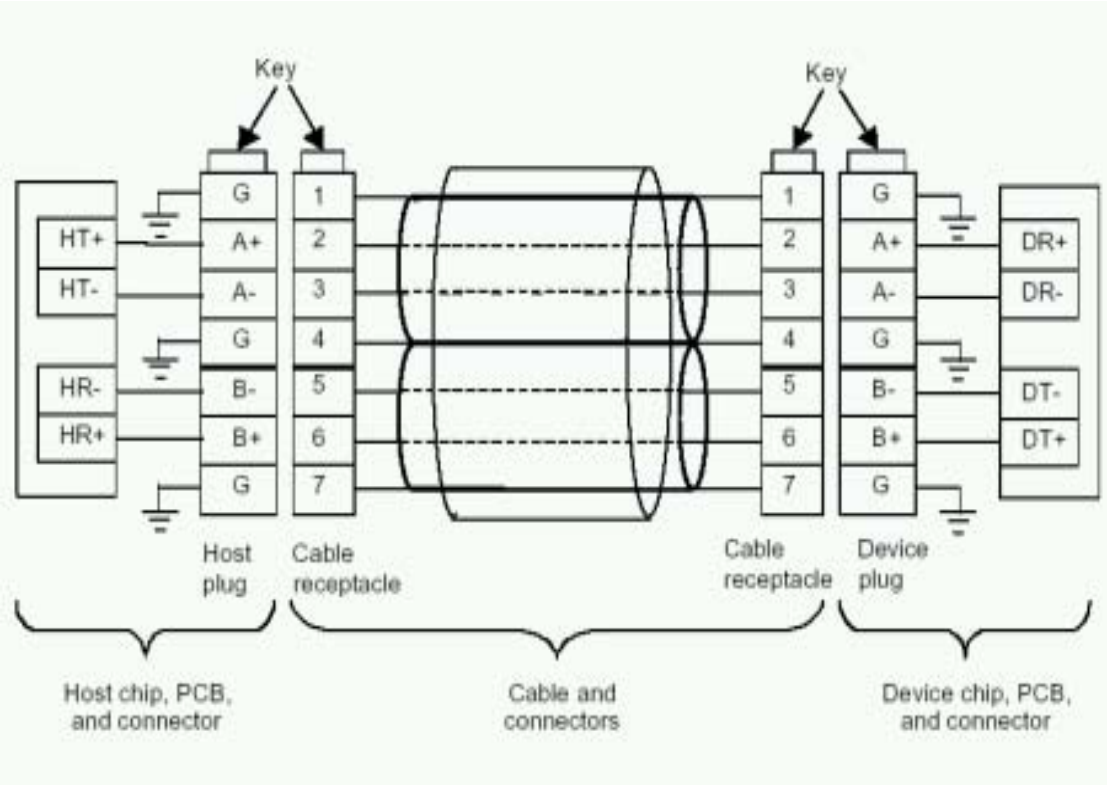
SATA とATA/ATAPI の比較

	ATA/ATAPI	Serial ATA
最大転送レート	133M Bytes/s	150M Bytes/s (1.5 Gbit/s)
ケーブルの信号ピン数	40pin/ 80pin	7 pin
ケーブルあたりの接続台数	2 (Shared Bus)	1(Point-to-Point 接続)
ケーブル長	18 inches	1m (内蔵用)
信号振幅	5 V	500mV
CRC Check	No(control) Yes(Data)	Yes

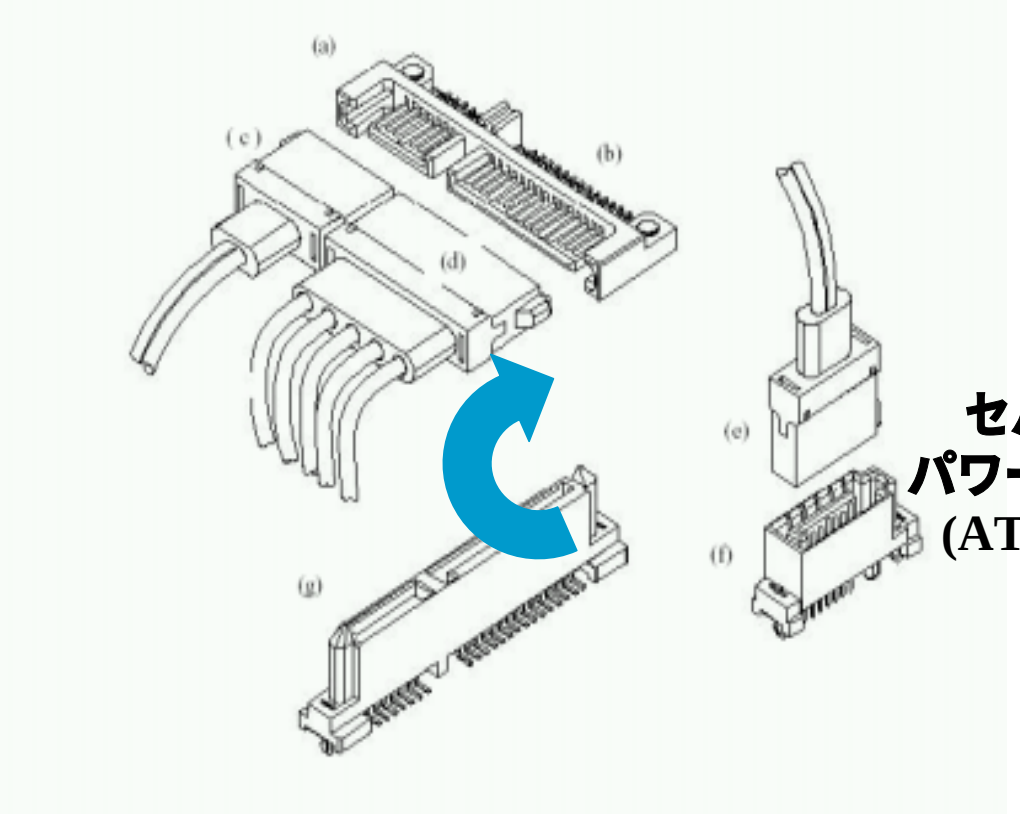
Serial ATA のLayered Architecture



SerialATA ケーブルの構造



Serial ATA のコネクタ構造



セパレート
パワー・コネクタ
(ATAと同じ)

SATAケーブル･コネクタの電気特性

差動インピーダンス

コネクタ	ケーブル
100 ohm ± 15%	100ohm ± 10% (最初の500ps)

ケーブルペアマッチング ± 5ohm

SATAの信号レベル

200mV - 300mV pp

400mV - 600mV ppd @TX

325mV - 600mV ppd @RX

OOB Signaling

OOB はOut-of-Band の略で、初期化･転送速度のネゴ･信号のresetを行なうためのハンドシェークである。

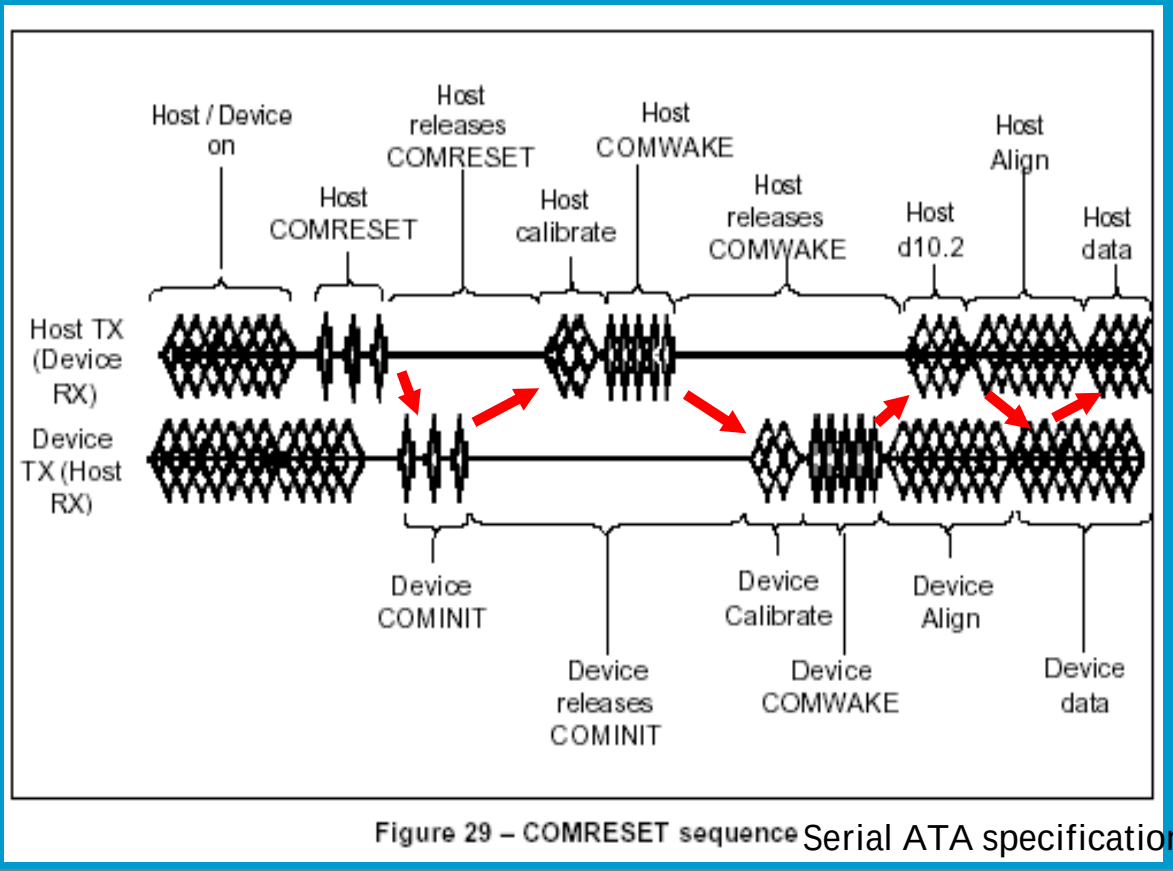


Figure 29 – COMRESET sequence Serial ATA specification Revision1.0より

Serial ATA OOB signals

OOB(Out-Of-Band) 信号が規定されている

COMRESET

Host が発生、Device に対する RESET 信号

COMINIT

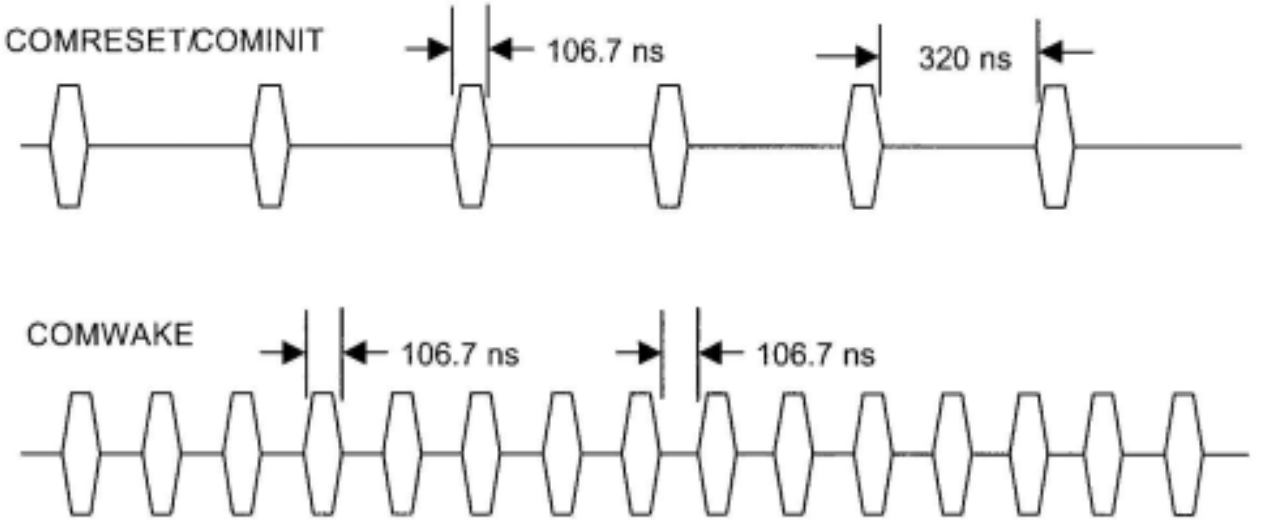
Device が発生、コミュニケーションの初期化信号

COMWAKE

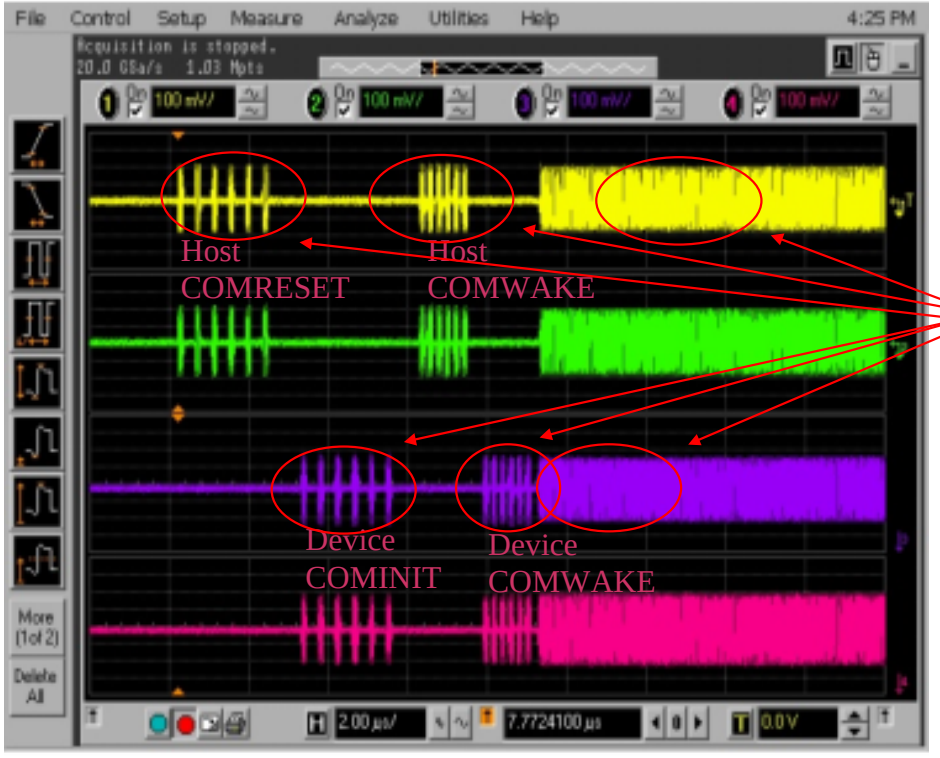
Host, Device が発生

Serial ATA OOB signals

COMRESET/COMINIT とCOMWAKE は同じALIGN Primitiveを使用している。異なるのはパケット間のgapである。



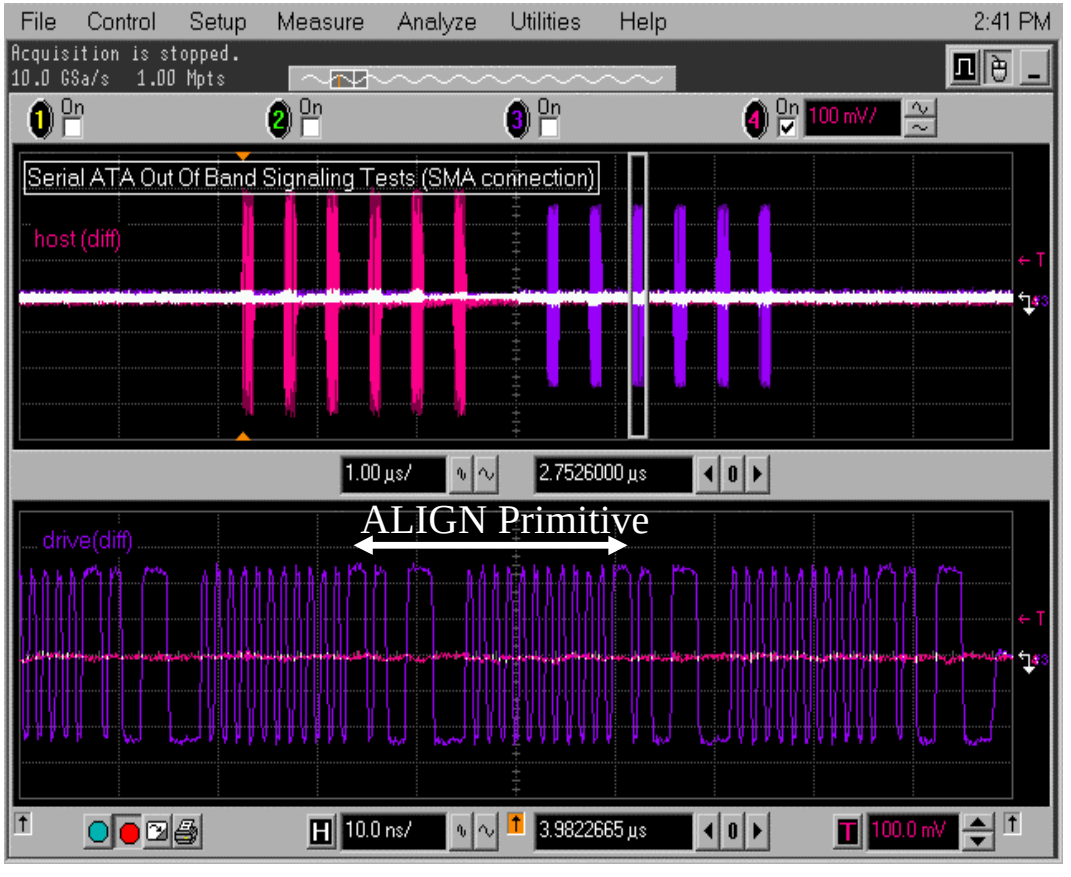
電源投入時の通信の様子



Align Primitiveが使われている

Single-end Probe でTx, RXの各差動ペア (計4本) を測定

COMRESET / COMINIT



Serial ATA 8B/10B Coding

8B/10B Encoding の目的はクロックシグナルをデータストリームに埋め込むこと。

0,1の数がほぼ同じで、DCバランスが保て、AC Coupling を可能に。

データコード(Dコード、8 bit)はすべての256 個のdata byteとして 10 bit に符号化。

Name	abcdei fghj output		Description
	Current rd-	Current rd+	
K28.3	001111 0011	110000 1100	Occurs only at byte 0 of all primitives except for the ALIGN primitive
K28.5	001111 1010	110000 0101	Occurs only at byte 0 of the ALIGN primitive

K-キャラクタは K28.3, K28.5 のみを使用

Serial ATA の8B10B Encoding

Byte notation	BCh, control character		4Ah, data character	
Bit notation	76543210	Control variable	76543210	Control variable
	10111100	K	01001010	D
Unencoded bit notation	HGF EDCBA	Z	HGF EDCBA	Z
	101 11100	K	010 01010	D
Bit notation reordered to conform with Zxx.y convention	Z EDCBA HGF		Z EDCBA HGF	
	K 11100 101		D 01010 010	
Character name	K 28 .5		D 10 .2	

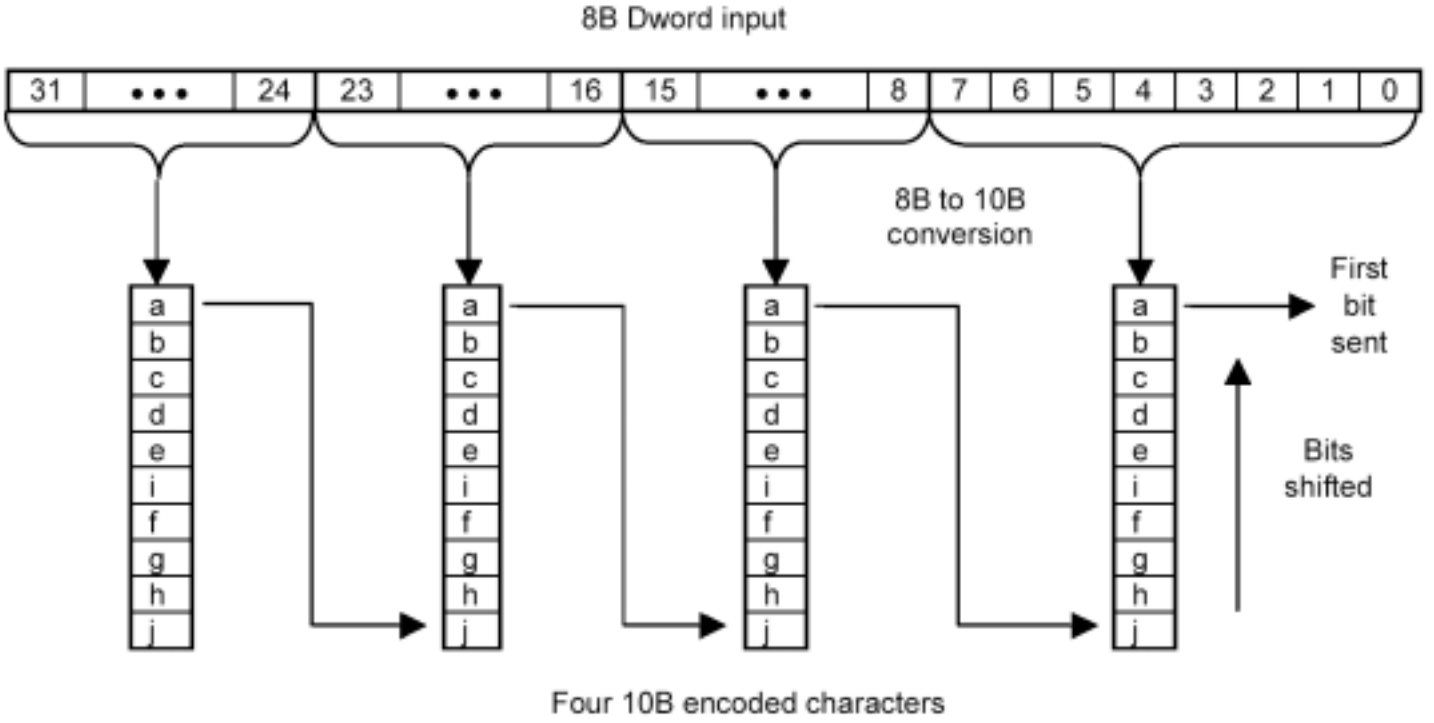
5B/6B 3B/4B**符号化**

5B/6B 3B/4B**符号化**

K28.5	001111 1010	110000 0101	
D10.2	4Ah	010101 0101	010101 0101

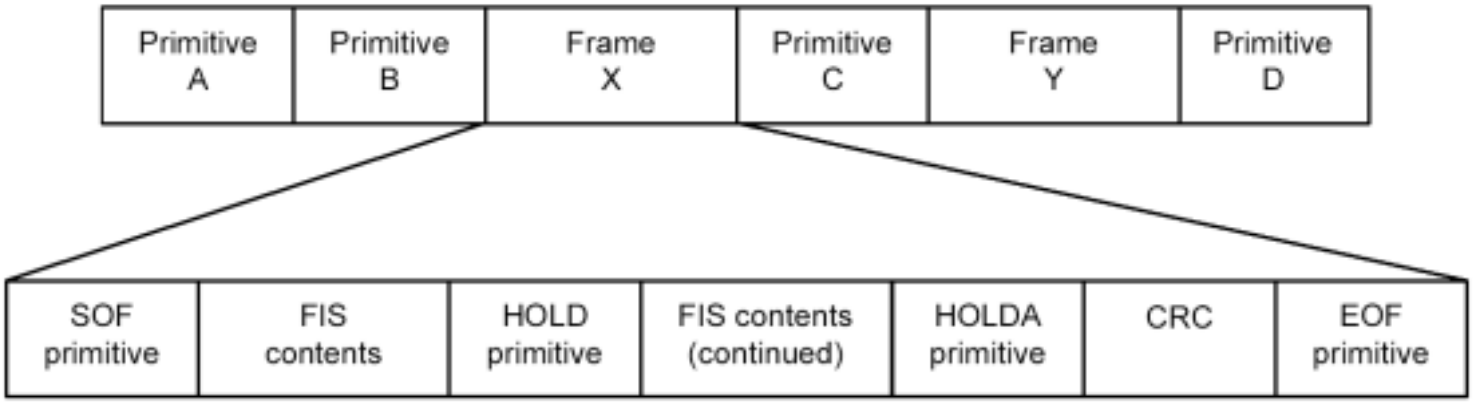
Transmission Bit Order

4バイト → Dword



ファイバ・チャネルと同じ

Transmission Structure



Serial ATA Primitives -Dwords-

Primitive name	Byte 3 contents	Byte 2 contents	Byte 1 contents	Byte 0 contents
ALIGN	D27.3	D10.2	D10.2	K28.5
CONT	D25.4	D25.4	D10.5	K28.3
DMAT	D22.1	D22.1	D21.5	K28.3
EOF	D21.6	D21.6	D21.5	K28.3
HOLD	D21.6	D21.6	D10.5	K28.3
HOLDA	D21.4	D21.4	D10.5	K28.3
PMACK	D21.4	D21.4	D21.4	K28.3
PMNAK	D21.7	D21.7	D21.4	K28.3
PMREQ_P	D23.0	D23.0	D21.5	K28.3
PMREQ_S	D21.3	D21.3	D21.4	K28.3
R_ERR	D22.2	D22.2	D21.5	K28.3
R_IP	D21.2	D21.2	D21.5	K28.3
R_OK	D21.1	D21.1	D21.5	K28.3
R_RDY	D10.2	D10.2	D21.4	K28.3
SOF	D23.1	D23.1	D21.5	K28.3
SYNC	D21.5	D21.5	D21.4	K28.3
WTRM	D24.2	D24.2	D21.5	K28.3
X_RDY	D23.2	D23.2	D21.5	K28.3

Serial ATA Primitives -1-

Primitive	Name	Description
ALIGN	Physical layer control	Upon receipt of an ALIGN, the physical layer readjusts internal operations as necessary to perform its functions correctly. This primitive is always sent in pairs - there is no condition where an odd number of ALIGN primitives shall be sent (except as not
CONT	Continue repeating previous primitive	The CONT primitive allows long strings of repeated primitives to be eliminated. The CONT primitive implies that the previously received primitive be repeated as long as another primitive is not received.
DMAT	DMA terminate	This primitive is sent as a request to the transmitter to terminate a DMA data transmission early by computing a CRC on the data sent and ending with a EOF primitive. The transmitter context is assumed to remain stable after the EOF primitive has been sen
EOF	End of frame	EOF marks the end of a frame. The previous non-primitive Dword is the CRC for the frame.
HOLD	Hold data transmission	HOLD is transmitted in place of payload data within a frame when the transmitter does not have the next payload data ready for transmission. HOLD is also transmitted on the backchannel when a receiver is not ready to receive additional payload data.
HOLDA	Hold acknowledge	This primitive is sent by a transmitter as long the HOLD primitive is received by its companion receiver.

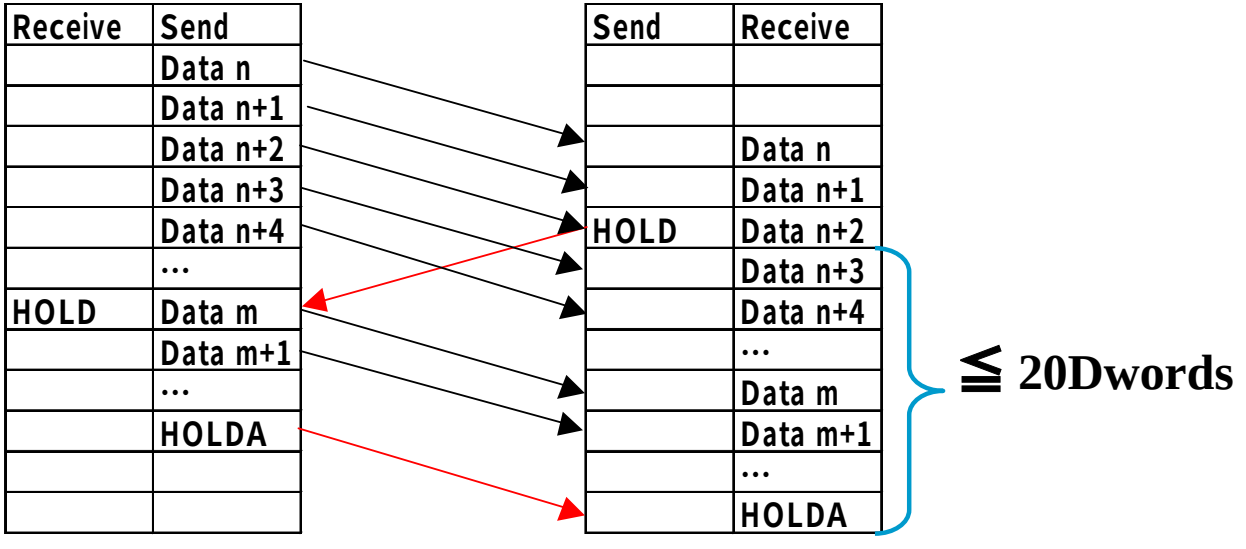
Serial ATA Primitives -2-

Primitive	Name	Description
PMACK	Power management acknowledge	Sent in response to a PMREQ_S or PMREQ_P when a receiving node is prepared to enter a power mode state.
PMNAK	Power management denial	Sent in response to a PMREQ_S or PMREQ_P when a receiving node is not prepared to enter a power mode state or when power management is not supported.
PMREQ_P	Power management request to partial	This primitive is sent continuously until PMACK or PMNAK is received. When PMACK is received, current node (host or device) will stop PMREQ_P and enters the Partial power management state.
PMREQ_S	Power management request to Slumber	This primitive is sent continuously until PMACK or PMNAK is received. When PMACK is received, current node (host or device) will stop PMREQ_S and enters the Slumber power management state.
R_ERR	Reception error	Current node (host or device) detected error in received payload.
R_IP	Reception in Progress	Current node (host or device) is receiving payload.
R_OK	Reception with no error	Current node (host or device) detected no error in received payload.
R_RDY	Receiver ready	Current node (host or device) is ready to receive payload.
SOF	Start of frame	Start of a frame. Payload and CRC follow to EOF.
SYNC	Synchronization	Synchronizing primitive always idle.
WTRM	Wait for frame termination	After transmission of any of the EOF, the transmitter will transmit WTRM while waiting for reception status from receiver.
X_RDY	Transmission data ready	Current node (host or device) has payload ready for transmission

Flow Control

HOLD: Stop sending data

HOLDA: Accept HOLD



CONT

同じデータパターンの繰り返しは EMI に不利

同じ Primitive の繰り返しを避けたい

同じ Primitive が続く時

CONT Primitive を送る

その後はスクランブルデータを送る

次の Primitive まで

FIS (Frame Information Structure)

SOF + Payload + EOF

Payload: FIS Type + Data + CRC ≦ 2064 Dwords

Register Type

Setup Type

Data Type

FIS Type -Location-

Byte 0

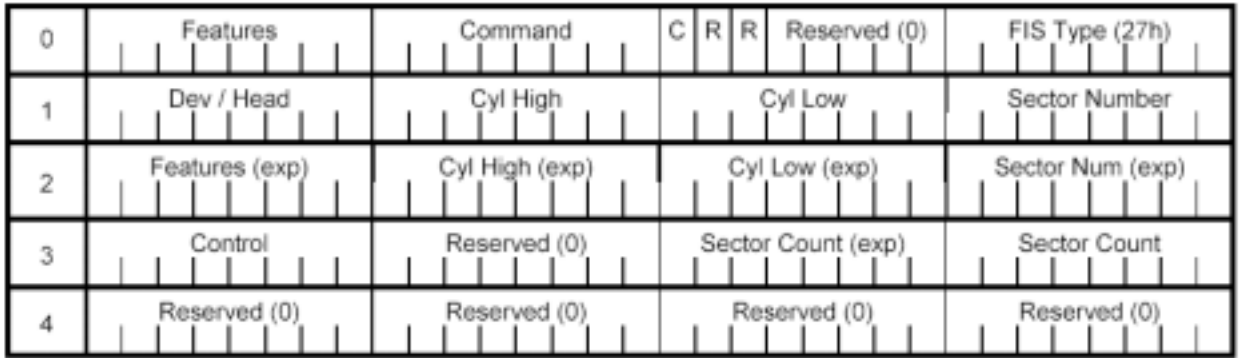
0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Features (exp)	Cyl High (exp)	Cyl Low (exp)				Sector Num (exp)
3	Control	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)

Register Type (Host to Device)

FIS Type

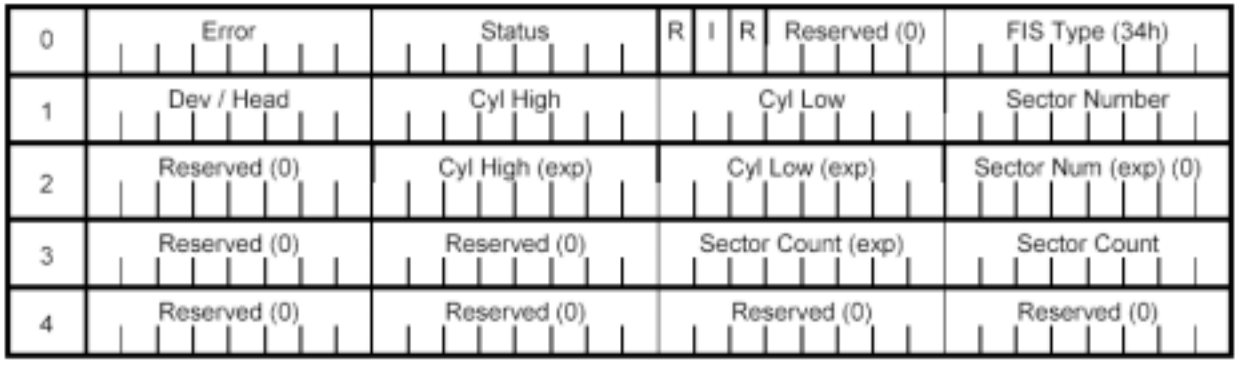
DESCRIPTION	DIRECTION	VALUE
Register	Host To Device	0x27
Register	Device To Host	0x34
Set Device Bit	Device to Host	0xA1
DMA Activate	Device to Host	0x39
DMA Setup	Device to Host	0x41
BIST Activate	Bidirectional	0x58
PIO Setup	Device to Host	0x5F
Data	Host to Device Device to Host	0x46

FIS -1-



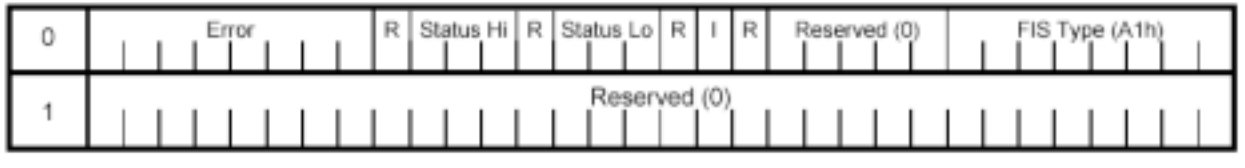
0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Features (exp)	Cyl High (exp)	Cyl Low (exp)				Sector Num (exp)
3	Control	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)

Register H to D



0	Error	Status	R	I	R	Reserved (0)	FIS Type (34h)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Reserved (0)	Cyl High (exp)	Cyl Low (exp)				Sector Num (exp) (0)
3	Reserved (0)	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)

Register D to H

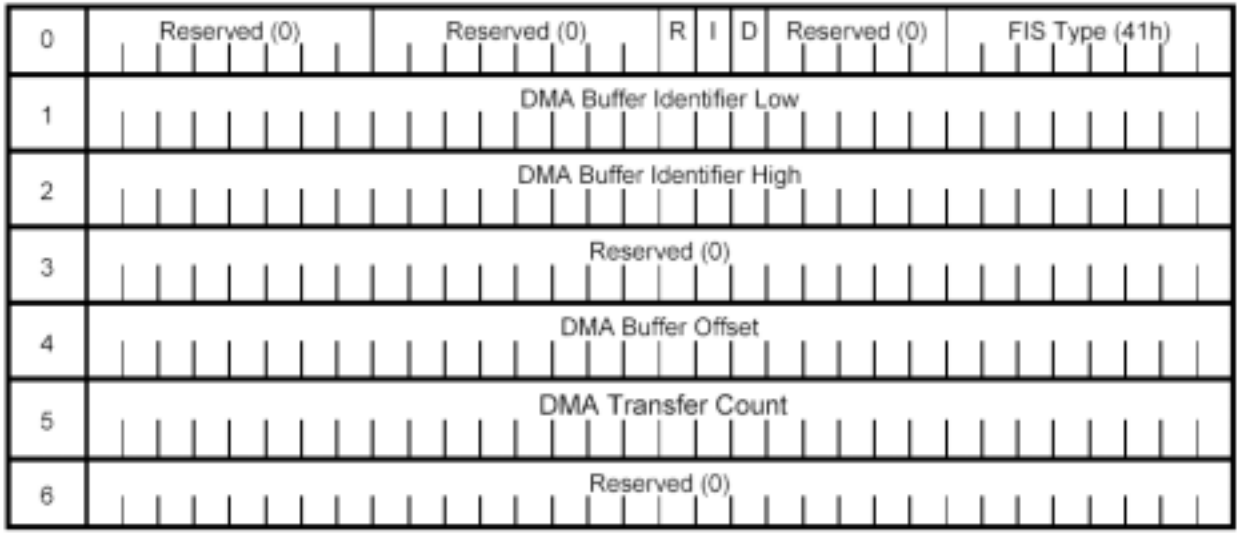


0	Error	R	Status Hi	R	Status Lo	R	I	R	Reserved (0)	FIS Type (A1h)
1	Reserved (0)									

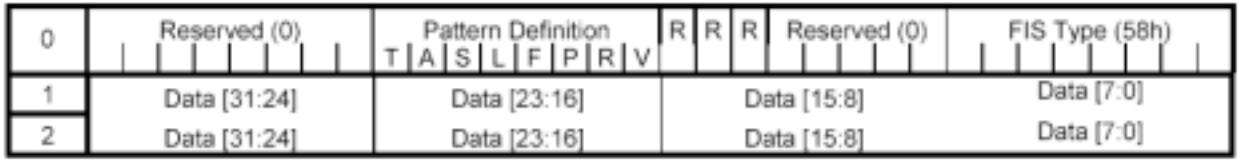
Set Device Bit

FIS -2-

DMA Active

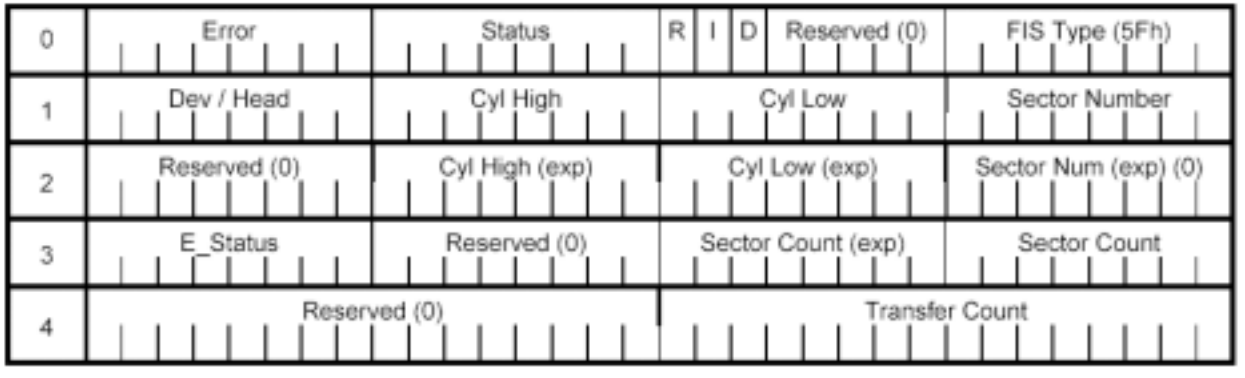


DMA Setup



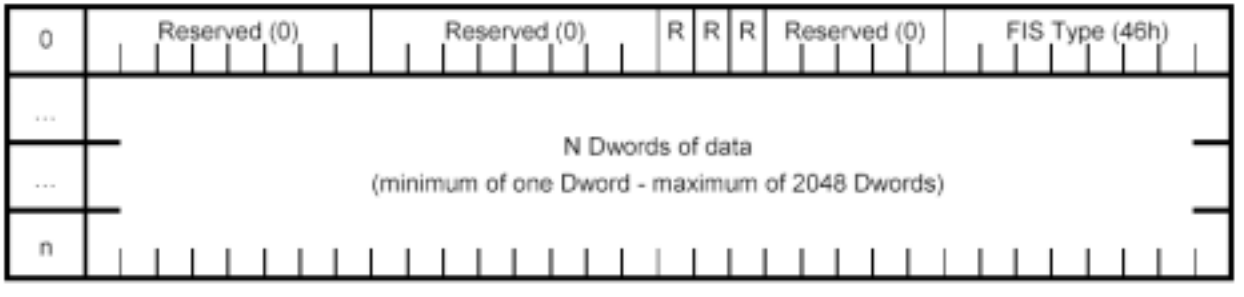
BIST Active

FIS -3-



0	Error	Status	R	I	D	Reserved (0)	FIS Type (5Fh)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Reserved (0)	Cyl High (exp)	Cyl Low (exp)				Sector Num (exp) (0)
3	E_Status	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)		Transfer Count				

PIO Setup



0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (46h)
...	N Dwords of data (minimum of one Dword - maximum of 2048 Dwords)						
...							
n							

Data

CRC

32bit CRC が使用されている

EOF の直前に位置する

式はファイバ･チャネルと同じ

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

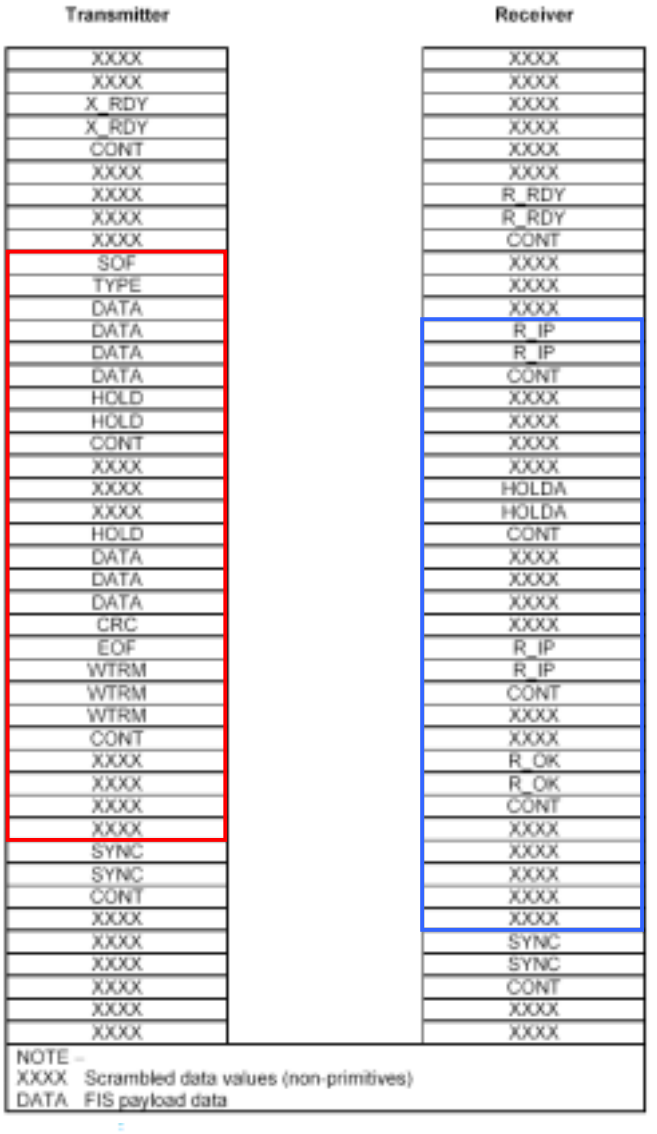
Frame Reception

R_IP: Frame を受信中

R_OK: Frame を正しく受信した

R_ERR: Frame 受信中にエラーを検出した

Frame Transmission Example



Transmitter	Receiver
XXXX	XXXX
XXXX	XXXX
X_RDY	XXXX
X_RDY	XXXX
CONT	XXXX
XXXX	XXXX
XXXX	R_RDY
XXXX	R_RDY
XXXX	CONT
SOF	XXXX
TYPE	XXXX
DATA	XXXX
DATA	R_IP
DATA	R_IP
DATA	CONT
HOLD	XXXX
HOLD	XXXX
CONT	XXXX
XXXX	XXXX
XXXX	HOLDA
XXXX	HOLDA
HOLD	CONT
DATA	XXXX
DATA	XXXX
DATA	XXXX
CRC	XXXX
EOF	R_IP
WTRM	R_IP
WTRM	CONT
WTRM	XXXX
CONT	XXXX
XXXX	R_OK
XXXX	R_OK
XXXX	CONT
XXXX	XXXX
SYNC	XXXX
SYNC	XXXX
CONT	XXXX
XXXX	XXXX
XXXX	SYNC
XXXX	SYNC
XXXX	CONT
XXXX	XXXX
XXXX	XXXX

NOTE –
XXXX Scrambled data values (non-primitives)
DATA FIS payload data

Serial ATA の将来動向

	Generation 1	Generation 2	Generation 3
Approximate speed (8b side)	1.2 Gbits/s (150 Mbytes/sec)	2.4 Gbits/s	4.8[1] Gbits/s
Approximate speed (10b side)	1.5 Gbits/sec	3.0 Gbits/sec	6.0[1] Gbits/sec
Estimated introduction date	mid 2001	mid 2004	mid 2007
Connector		Same as Gen 1	May be upgraded
Cable		Same as Gen 1	May be upgraded
Signaling compatibility		Compatible with Generation 1	Compatible with Generation 2 - may be compatible with Generation 1

NOTE –

1. These speed specifications and schedules are subject to change

参考文献

Serial ATA / High Speed Serialized AT Attachment specification (revision 1.0)

Serial ATA Storage Architecture and Applications (Intel Press)

Serial ATA Compliance Test Procedure

Serial ATA Motherboard Signal Quality Test Lab

(IDF Spring 2003)